REMARKS

Claims 1-10 are pending. Claim 4 has been amended to delete the phrase "an extremely short time," claim 6 has been amended for clarification, and claim 9 has been amended so as to depend from claim 1. No new matter has been added.

Applicants thank the Examiner and the Examiner's supervisor for the courtesy of hosting a brief telephone interview with applicants' representative on July 28, 2008, to discuss the double patenting issues raised in the Action. During the interview, the Examiner explained that all double patenting issues in the current Action relate to non-statutory double patenting and not statutory double patenting. That is, the Examiner has not found any of the pending claims to be identical to claims in other applications.

In the Action, the Examiner asserted that claims 1-3 and 5-6 conflict with claims 1-2 and 4 of U.S. Patent Application No. 10/590,225 ("the '225 application") and requested applicants to "either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822." Applicants respectfully traverse this requirement.

The language of the requirement is taken from form paragraph 8.29 of MPEP § 822, which is directed to "claims to inventions that are not distinct." (See, the title of MPEP § 822.) MPEP § 822 states that "[f]orm paragraph 8.29 should be used when the conflicting claims are *identical* or conceded by applicant to be not patentably distinct" (emphasis added). Currently pending claims 1-3 and 5-6 are not identical to claims 1-2 and 4 of the '225 application. For example, claims 1-2 and 4 of the '225 application recite a "coarse delay circuit," a feature not recited in any of claims 1-3 and 5-6 in the present application. Because claims 1-3 and 5-6 are not identical to claims 1-2 and 4 of the '225 application and applicants have not conceded that they are not patentably distinct, the Examiner's request to cancel claims is improper and should be withdrawn.

The Examiner provisionally rejected claims 1-3 and 6 on the ground of nonstatutory double patenting over claim 1 of the '225 application. Because there are currently other rejections in this case, applicants are not required to address the provisional rejection at this time. (See, MPEP § 804(I)(B)(1).)

The Examiner objected to claim 4 based on the phrase "an extremely short time." Applicants have amended claim 4 to obviate the objection.

The Examiner rejected claims 1-4, 7, and 10 under 35 USC § 102(b) as being anticipated by Matsuzaki, U.S. Patent No. 6,088,255. Applicants respectfully traverse this rejection.

Claim 1 recites "a means for inputting a first signal output during 1 clock cycle of the internal clock to the variable delay addition circuit through the dummy delay at a start of burst." Claim 1 further recites "a means for detecting duration time of an active logic value of the first signal input by the variable delay addition circuit through the dummy delay until the end of the 1 clock cycle of the internal clock and setting an initial value of delay amount of the variable delay addition circuit based on the duration time at the start of burst." Matsuzaki fails to disclose or suggest either of these features.

The Examiner asserts that both of these features are "inherent based on the structure of Matsuzaki's Figure 11." Applicants respectfully disagree.

The Examiner compares the second variable-delay circuit 220 of Matsuzaki with the claimed variable delay addition circuit. However, the second variable-delay circuit 220 of Matsuzaki does not inherently receive "a first signal output during 1 clock cycle of the internal clock...through a dummy delay at a start of burst." That is, nothing in the operation of the circuit of FIG. 11 of Matsuzaki requires second variable-delay circuit 220 to receive a first signal as claimed.

As shown in FIG. 11 of Matsuzaki, second variable-delay circuit 220 receives only two signals: a signal output by an input buffer 800 and a signal output by a delay control circuit 400. The Examiner has equated these two signals with the claimed variable delay addition circuit and

the claimed internal clock, respectively. However, the Examiner has presented no evidence that the second variable-delay circuit 220 of Matsuzaki must additionally receive the claimed first signal. Accordingly, the rejection of claim 1 should be withdrawn.

Moreover, the claimed "means for detecting duration time" and "setting an initial value of delay amount" are related to the claimed first signal and to the claimed burst, respectively. Neither the first signal nor the burst is disclosed in Matsuzaki, either inherently or explicitly. Accordingly, the rejection of claim 1 should be withdrawn for this reason as well.

Applicants respectfully submit that the Examiner has failed to provide adequate reasons to support a rejection based on inherency as set forth by the MPEP. MPEP § 2112 (IV) requires that:

> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original)

MPEP § 2112 (IV) further requires that:

> "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted)

In the present case, the Examiner provided only the following statement in support of the inherency rejection:

> Matsuzaki's specification teaches that both the dummy-input buffer 280 and the dummy-data-output buffer 290 have a delay value (column 25, lines 47-49), that the dummy-input buffer 280 has the same delay as the input buffer 800, and that the dummy-

> data-output buffer 290 has the same delay as the data-output buffer 900 (column 16, lines 1-9).

This statement does not provide the basis in fact or technical reasoning required for showing inherency. For example, the statement fails to demonstrate an inherent means for inputting a first signal at a start of a burst. In fact, the statement does not address the recited burst at all. Likewise, the statement fails to demonstrate an inherent means for detecting a duration time and setting an initial value of delay amount. Because the Examiner has failed to meet the burden required for a rejection based on inherency, the rejection of claim 1 should be withdrawn for this reason as well.

Claims 2 and 3 were rejected based on inherency arguments similar to those presented in relation to claim 1. Accordingly, the rejections of claims 2 and 3 should be withdrawn for reasons similar to those detailed above.

Claims 4 and 7 depend from claims 1-3 and overcome the current rejections for at least the reasons given above with respect to the parent claims.

The Action states, on page 7, that claim 10 is rejected over Makino. However, upon reviewing the rejection (and in particular the reference numbers cited in the rejection), it appears that the Examiner intended to reject claim 10 over Matsuzaki rather than Makino. Specifically, applicants believe that the Examiner intended to reject claim 10 based on the disclosure in Matsuzaki of the phase-comparison unit 25 shown in Figure 5. Therefore, in responding to the rejection, applicants will assume that the rejection of claim 10 is a rejection under 35 USC § 102(b) over Figure 5 of Matsuzaki.

Claim 10 recites "latching [a] delay signal at [a] time when [a] clocked inverter is disabled by a reference clock." Figure 5 of Matsuzaki fails to disclose or suggest a similar feature.

The Examiner compares signal S2 of Matsuzaki with the claimed delay signal and compares signal S1 of Matsuzaki with the claimed reference clock. The Examiner further

compares NAND gate 36 of Matsuzaki with the claimed clocked inverter and explains that NAND gate 36 is disabled when signal S1 is low. The Examiner then concludes that signal S2 is latched by first and second latches (corresponding to NAND gates 41-42 and 43-44, respectively) when the NAND gate 36 is disabled by signal S1. Applicants respectfully submit that this conclusion is incorrect.

When signal S1 is low, the output of NAND gate 36 goes high. As a result, the output of NOR gate 49 goes low. In response to the low output of NOR gate 49, the respective outputs of NAND gates 37-40 all go high. When the respective outputs of NAND gates 37-40 are all high due to signal S1, the logic level of signal S2 does not affect the values latched in the first and second latches. In other words, the logic level of signal S2 is not latched by the first and second latches when NAND gate 36 is disabled by signal S1. Because the circuit in Figure 5 of Matsuzaki does not behave as explained by the Examiner, the Examiner has failed to provide support for the rejection of claim 10. Accordingly, the rejection of claim 10 should be withdrawn.

Claim 8 stands rejected under 35 USC § 102(b) as being anticipated by Kikuda, U.S. Patent No. 4,914,326. Applicants respectfully traverse this rejection.

Claim 8 recites "[a] delay element comprising an inverter an a transfer gate, wherein variations in delay time due to variations in power supply voltage can be minimized by supplying electric potential having dependency opposite to increase and decrease in power source voltage to a gate input of the transfer gate." Kikuda fails to disclose a delay element as claimed.

The Examiner compares Figure 5 of Kikuda with the claimed delay element. Figure 5 of Kikuda shows a delay circuit having a transmission gate 20 and an inverter circuit 10. However, because of the way that transmission gate 20 and inverter circuit 10 of Kikuda are connected to each other, a gate of transmission gate 20 does not receive an "electric potential having dependency opposite to increase and decrease in power source voltage," as recited in claim 8. In

particular, in Kikuda, the gates of transmission gate 20 receive the output voltage of inverter 10, which is equal to either power source voltage Vcc or ground. Thus, the gate voltages in Kikuda do not vary with a dependency opposite to increases or decreases in the power source voltage. Because Kikuda does not disclose a delay element having the voltage relationship as claimed, the rejection of claim 8 should be withdrawn.

Claims 6 and 9 stand rejected under 35 USC § 103(a) as being unpatentable over Matsuzaki and Makino, U.S. Patent No. 4,820,843, respectively. As currently amended, claims 6 and 9 depend from one of claims 1 through 3. Accordingly claims 6 and 9 overcome the corresponding rejections for at least the reasons given above with respect to the parent claims.

Early action allowing the claims in this application is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing 559502005300.

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